FIG.1

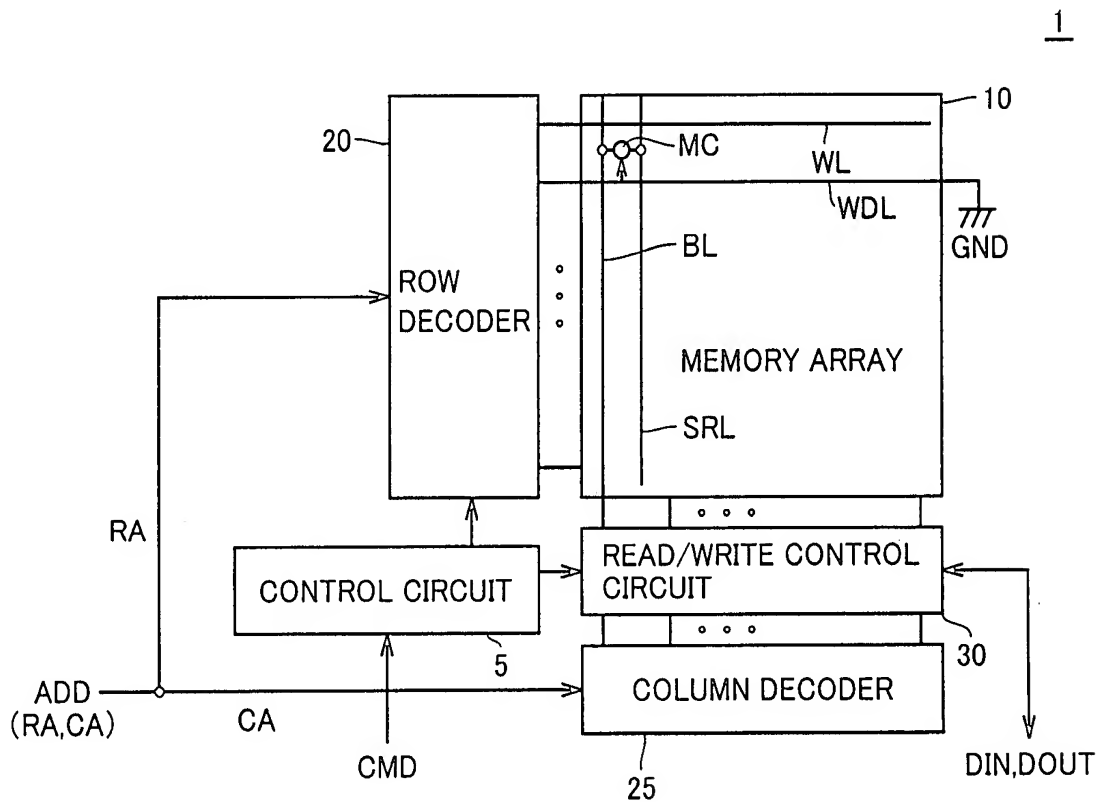
1
10
20
MC
WL
WDL
GND
BL
ROW
DECODER
MEMORY ARRAY
SRL
RA
CONTROL CIRCUIT
READ/WRITE CONTROL
CIRCUIT
30
5
ADD
(RA,CA)
CA
COLUMN DECODER
CMD
25
DIN,DOUT

FIG.2

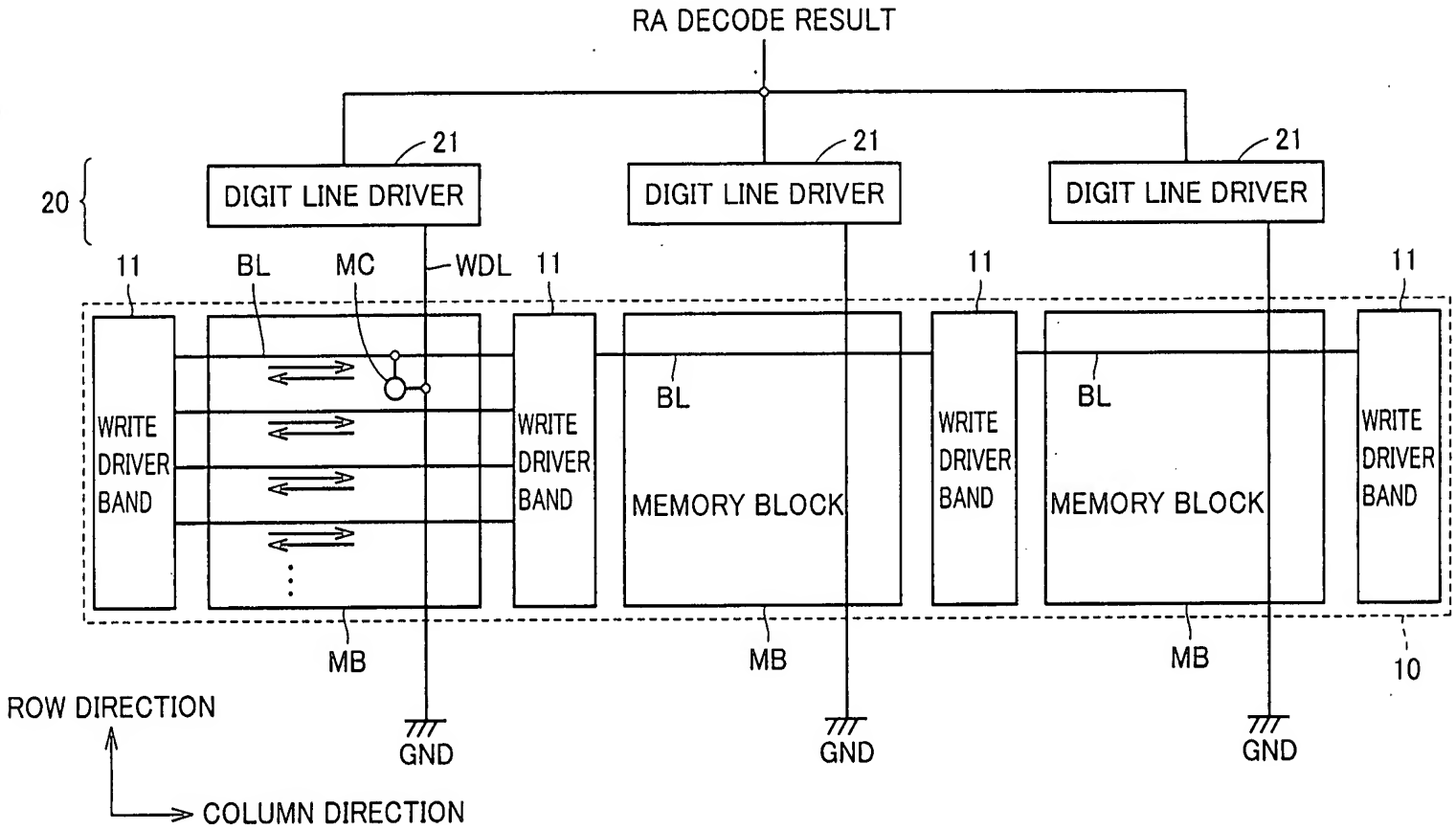
RA DECODE RESULT
20
21
DIGIT LINE DRIVER
21
DIGIT LINE DRIVER
21
DIGIT LINE DRIVER
11
BL
MC
WDL
11
11
11
WRITE DRIVER BAND
WRITE DRIVER BAND
BL
MEMORY BLOCK
WRITE DRIVER BAND
BL
MEMORY BLOCK
WRITE DRIVER BAND
MB
MB
MB
10
GND
GND
GND
ROW DIRECTION
COLUMN DIRECTION

FIG.3A

OPERATION OF WRITING DIFFERENT DATA THROUGH ADJACENT BLs

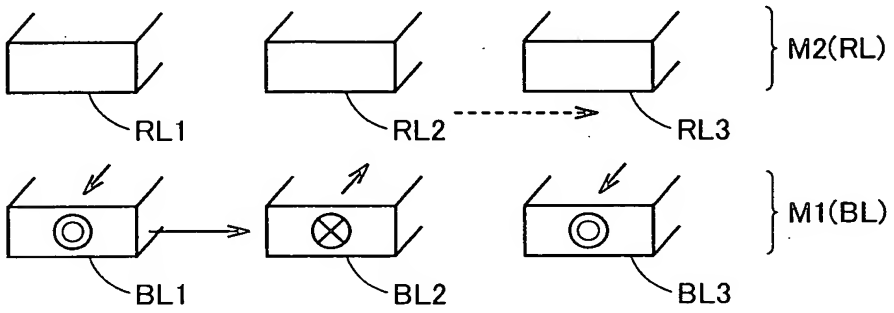

FIG.3B

OPERATION OF WRITING SAME DATA THROUGH ADJACENT BLs

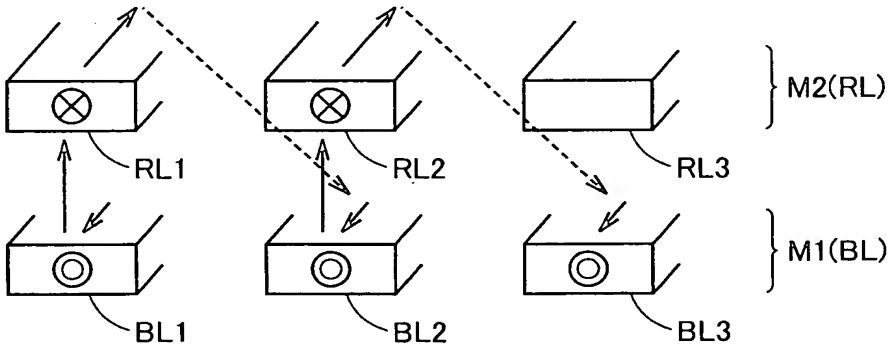

FIG.4

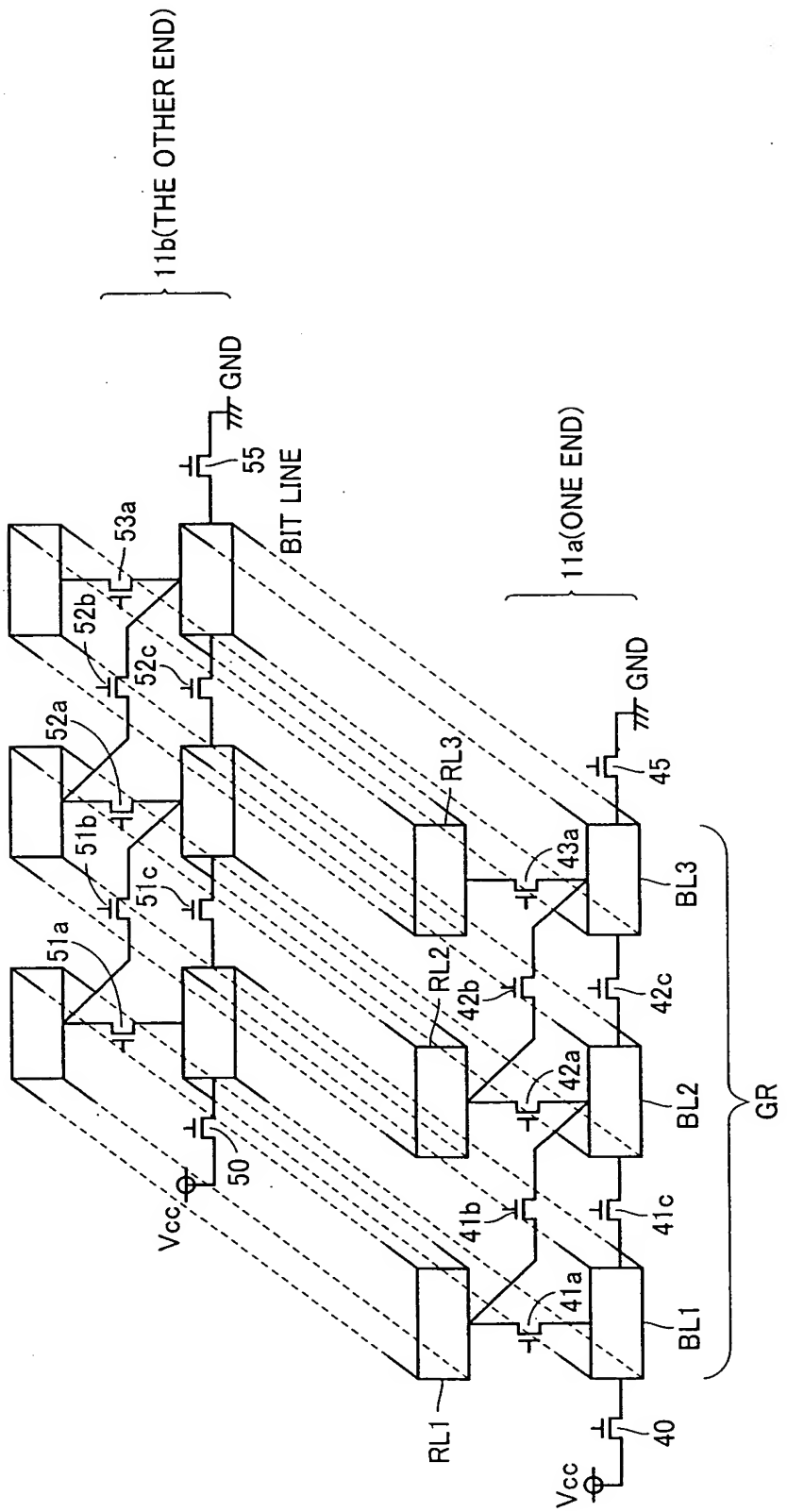
11b(THE OTHER END)
11a(ONE END)
GND
55
BIT LINE
53a
52b
52c
52a
51b
51c
51a
50
Vcc
RL1
RL2
RL3
41b
41c
41a
42b
42c
42a
43a
45
40
BL1
BL2
BL3
GR

FIG.5

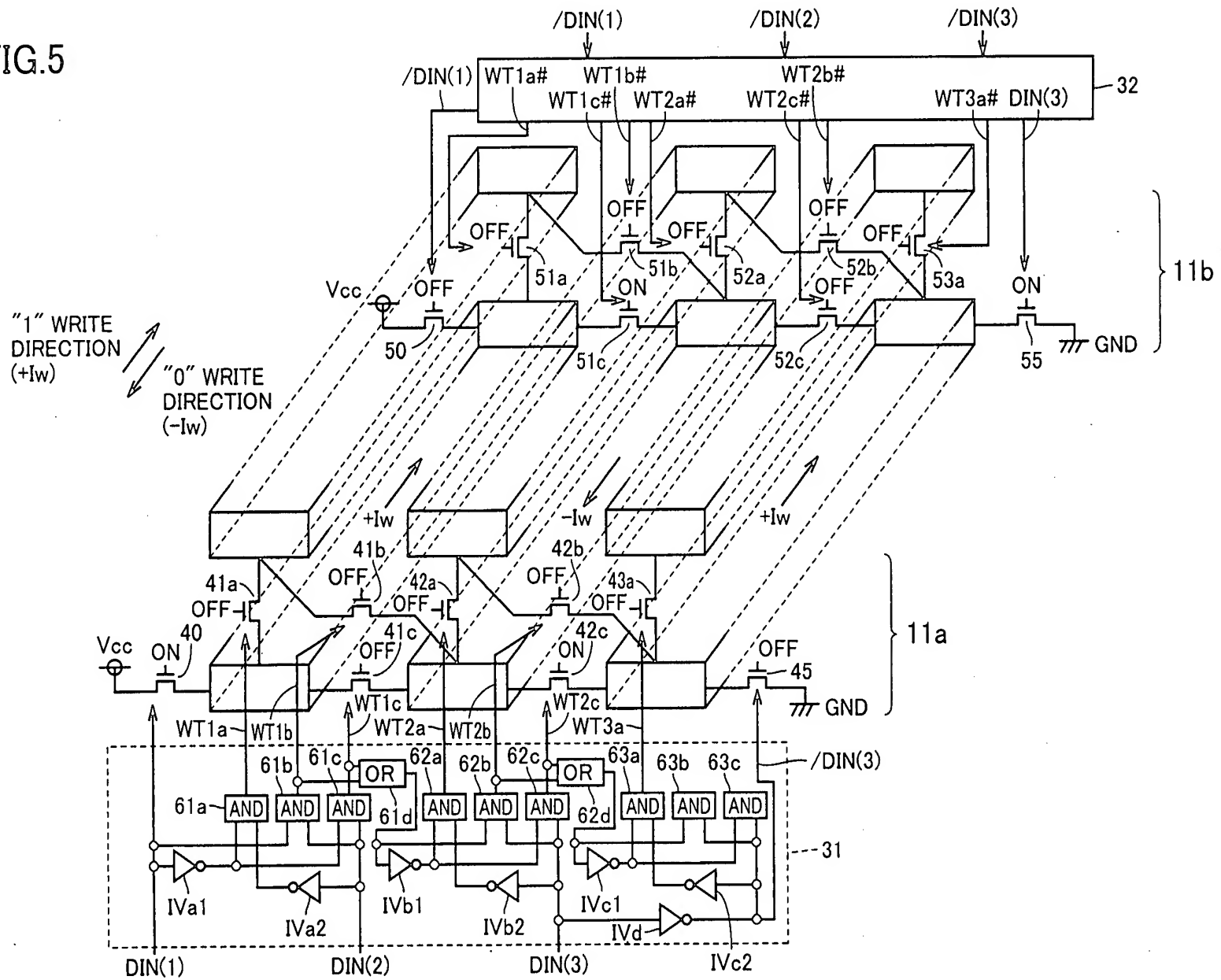
/DIN(1)
/DIN(2)
/DIN(3)
WT1a#
WT1b#
WT1c#
WT2a#
WT2b#
WT2c#
WT3a#
DIN(3)
32
OFF
ON
51a
51b
51c
52a
52b
52c
53a
55
50
Vcc
GND
11b
"1" WRITE DIRECTION (+Iw)
"0" WRITE DIRECTION (-Iw)
+Iw
-Iw
41a
41b
41c
42a
42b
42c
43a
40
45
11a
WT1a
WT1b
WT1c
WT2a
WT2b
WT2c
WT3a
61a
61b
61c
61d
62a
62b
62c
62d
63a
63b
63c
AND
OR
/DIN(3)
31
IVa1
IVa2
IVb1
IVb2
IVc1
IVc2
IVd
DIN(1)
DIN(2)
DIN(3)

FIG.6

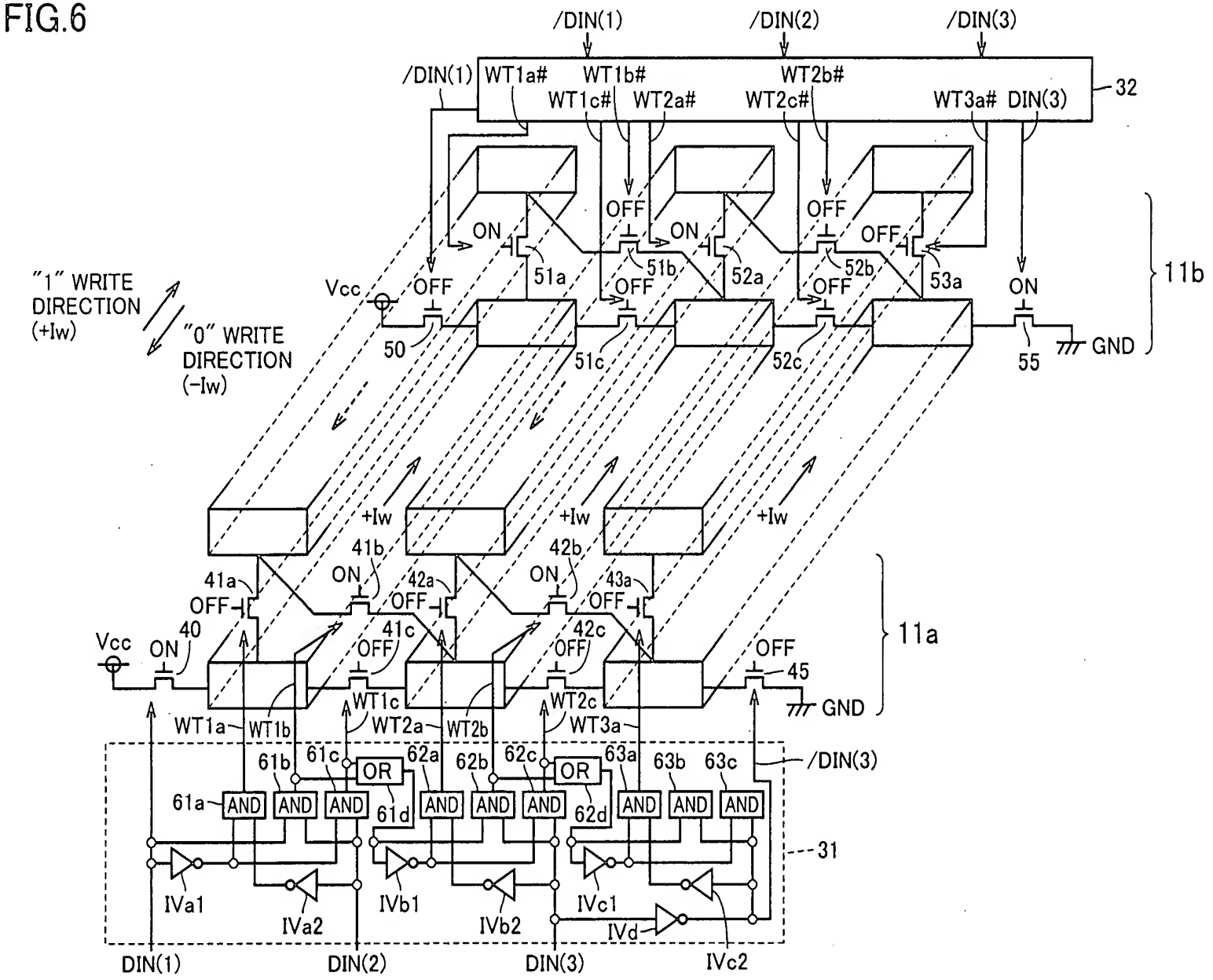
/DIN(1)
/DIN(2)
/DIN(3)
WT1a#
WT1b#
WT1c#
WT2a#
WT2b#
WT2c#
WT3a#
DIN(3)
32
ON
OFF
51a
51b
52a
52b
53a
11b
"1" WRITE DIRECTION (+Iw)
"0" WRITE DIRECTION (-Iw)
Vcc
50
51c
52c
55
GND
+Iw
41a
41b
42a
42b
43a
40
41c
42c
45
11a
WT1a
WT1b
WT1c
WT2a
WT2b
WT2c
WT3a
61a
61b
61c
61d
62a
62b
62c
62d
63a
63b
63c
AND
OR
31
IVa1
IVa2
IVb1
IVb2
IVc1
IVc2
IVd
DIN(1)
DIN(2)
DIN(3)

FIG.7

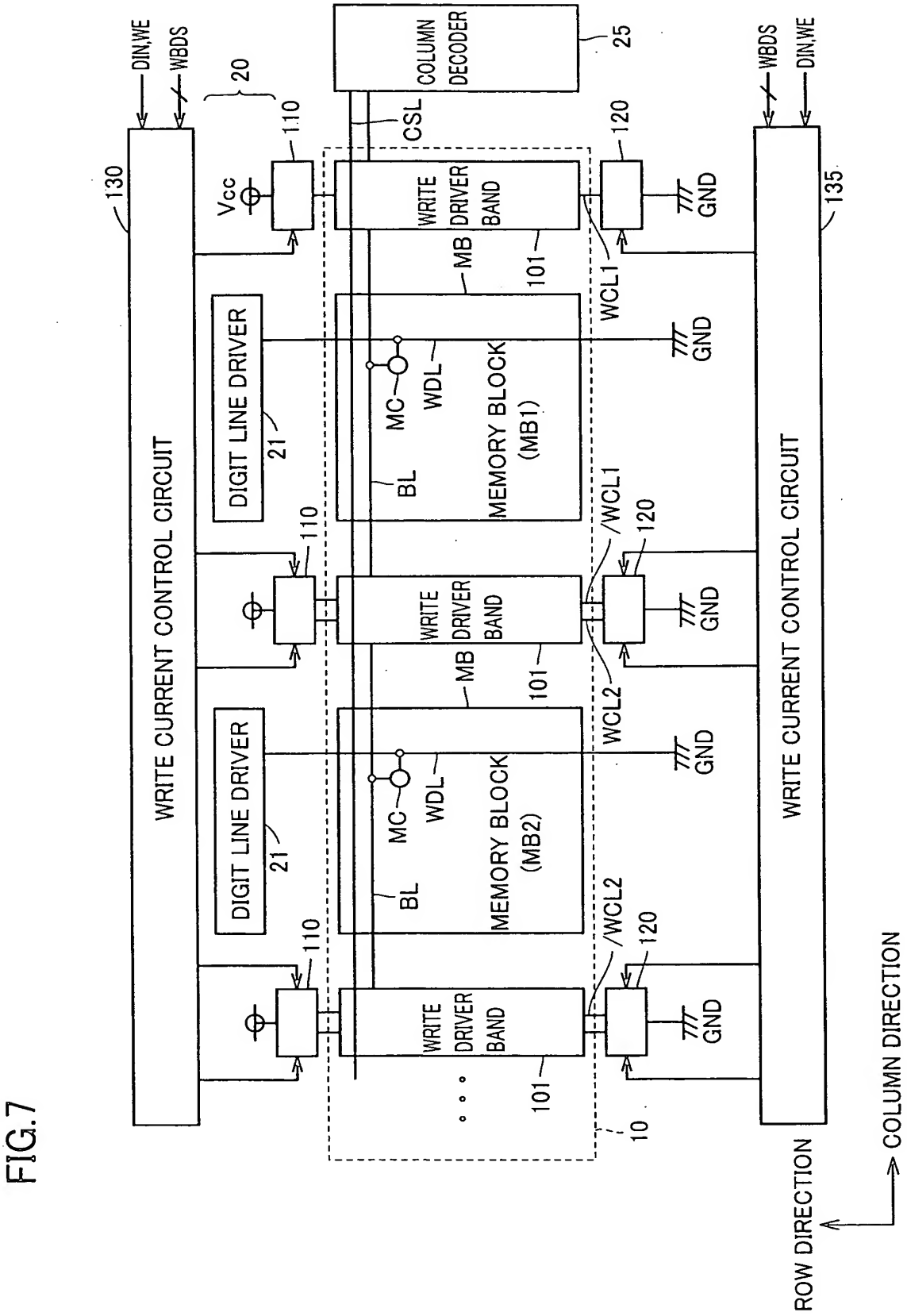
DIN,WE
WBDS
20
110
130
WRITE CURRENT CONTROL CIRCUIT
Vcc
COLUMN DECODER
25
CSL
120
WRITE DRIVER BAND
MB
101
WCL1
GND
135
DIGIT LINE DRIVER
21
MC
WDL
BL
MEMORY BLOCK (MB1)
/WCL1
WCL2
/WCL2
MEMORY BLOCK (MB2)
10
ROW DIRECTION
COLUMN DIRECTION

FIG.8

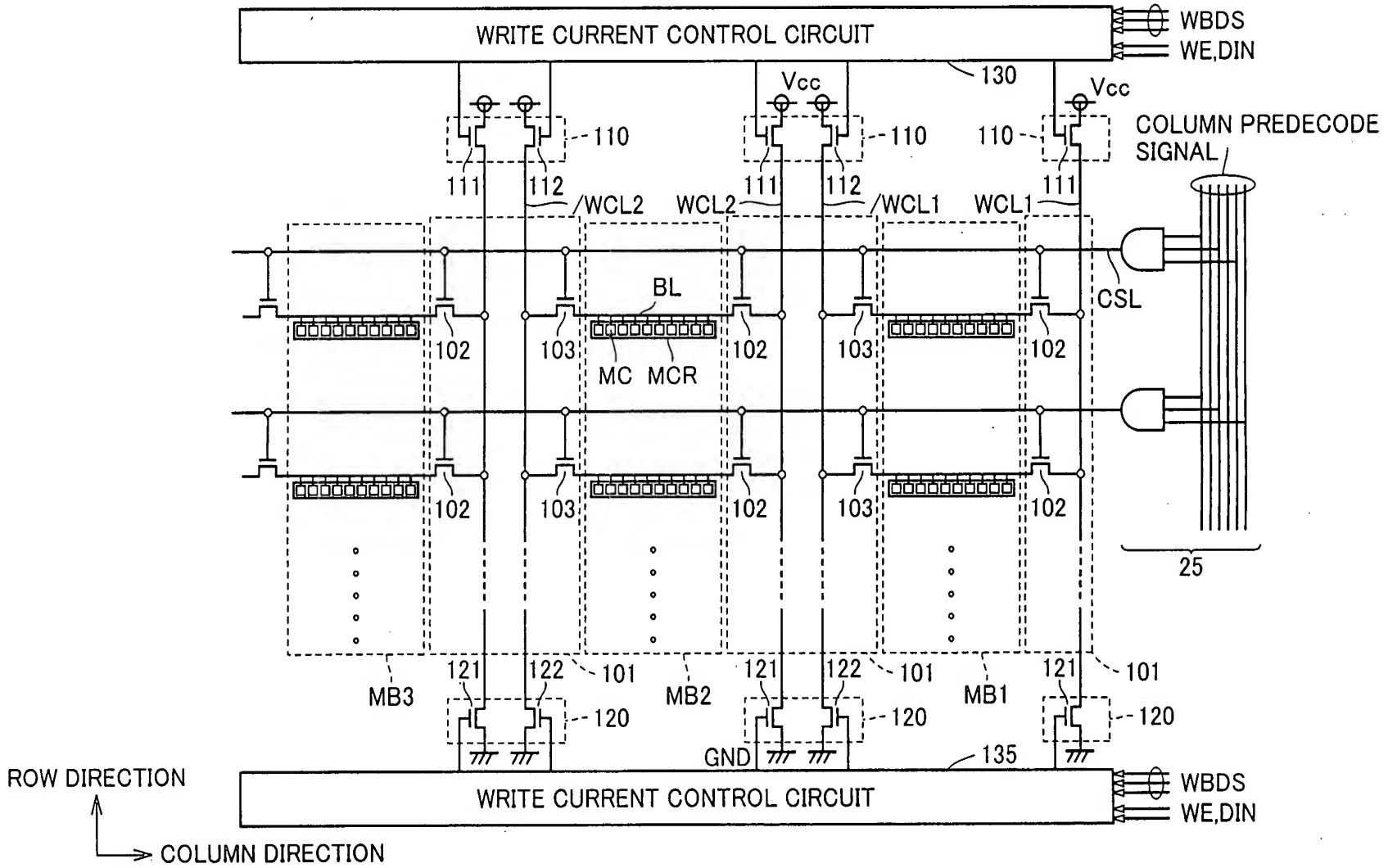
WRITE CURRENT CONTROL CIRCUIT
WBDS
WE,DIN
130
Vcc
Vcc
110
110
110
COLUMN PREDECODE SIGNAL
111
112
WCL2
WCL2
111
112
WCL1
WCL1
111
BL
CSL
102
103
MC
MCR
102
103
102
103
102
25
MB3
121
122
101
MB2
121
122
101
MB1
121
101
120
120
120
GND
135
WRITE CURRENT CONTROL CIRCUIT
WBDS
WE,DIN
ROW DIRECTION
COLUMN DIRECTION

FIG.9

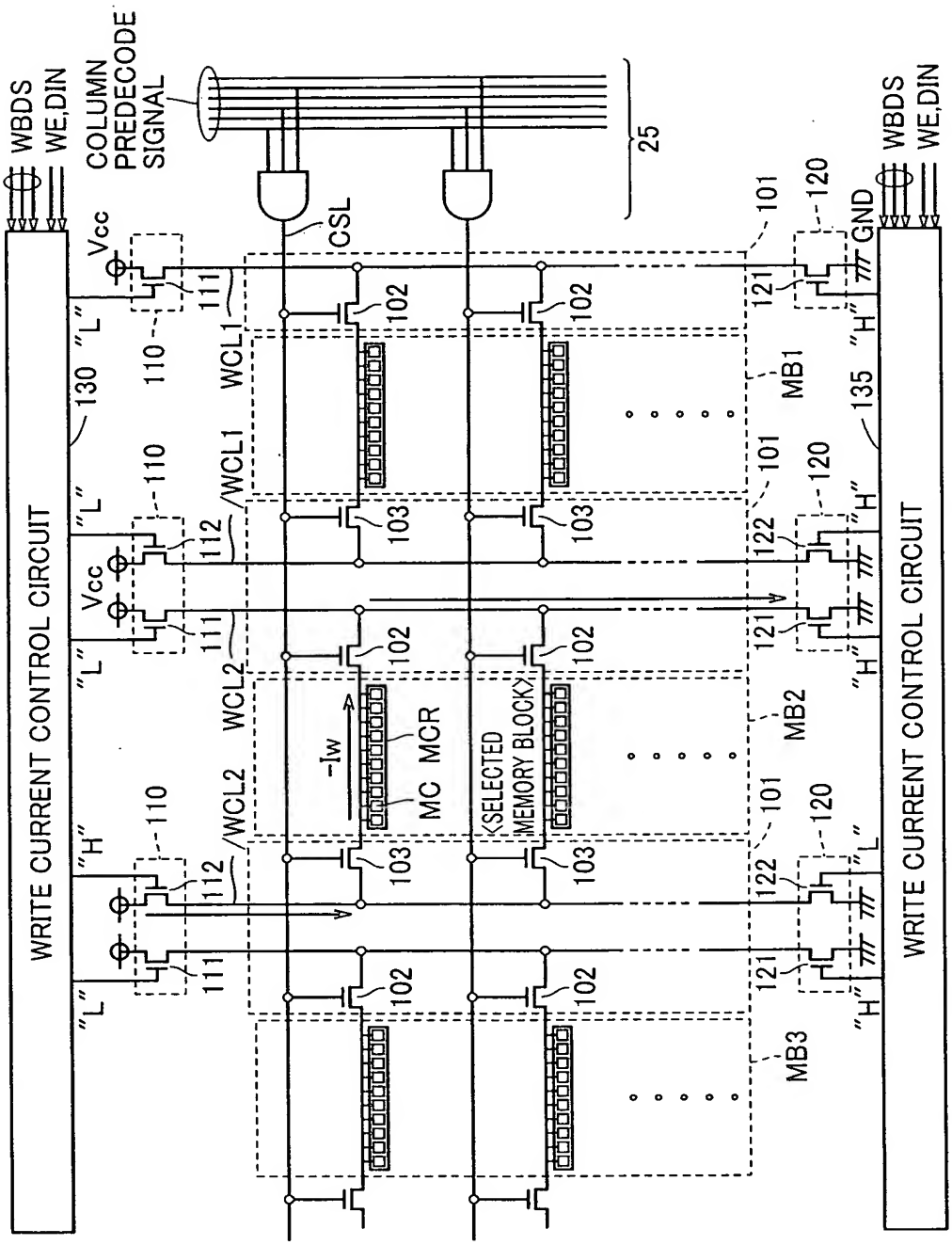
WBDS
WE,DIN
COLUMN PREDECODE SIGNAL
25
CSL
Vcc
GND
WRITE CURRENT CONTROL CIRCUIT
WRITE CURRENT CONTROL CIRCUIT
WCL1
/WCL1
WCL2
/WCL2
-Iw
MC
MCR
SELECTED MEMORY BLOCK
MB1
MB2
MB3
"H"
"L"
101
102
103
110
111
112
120
121
122
130
135

FIG.10

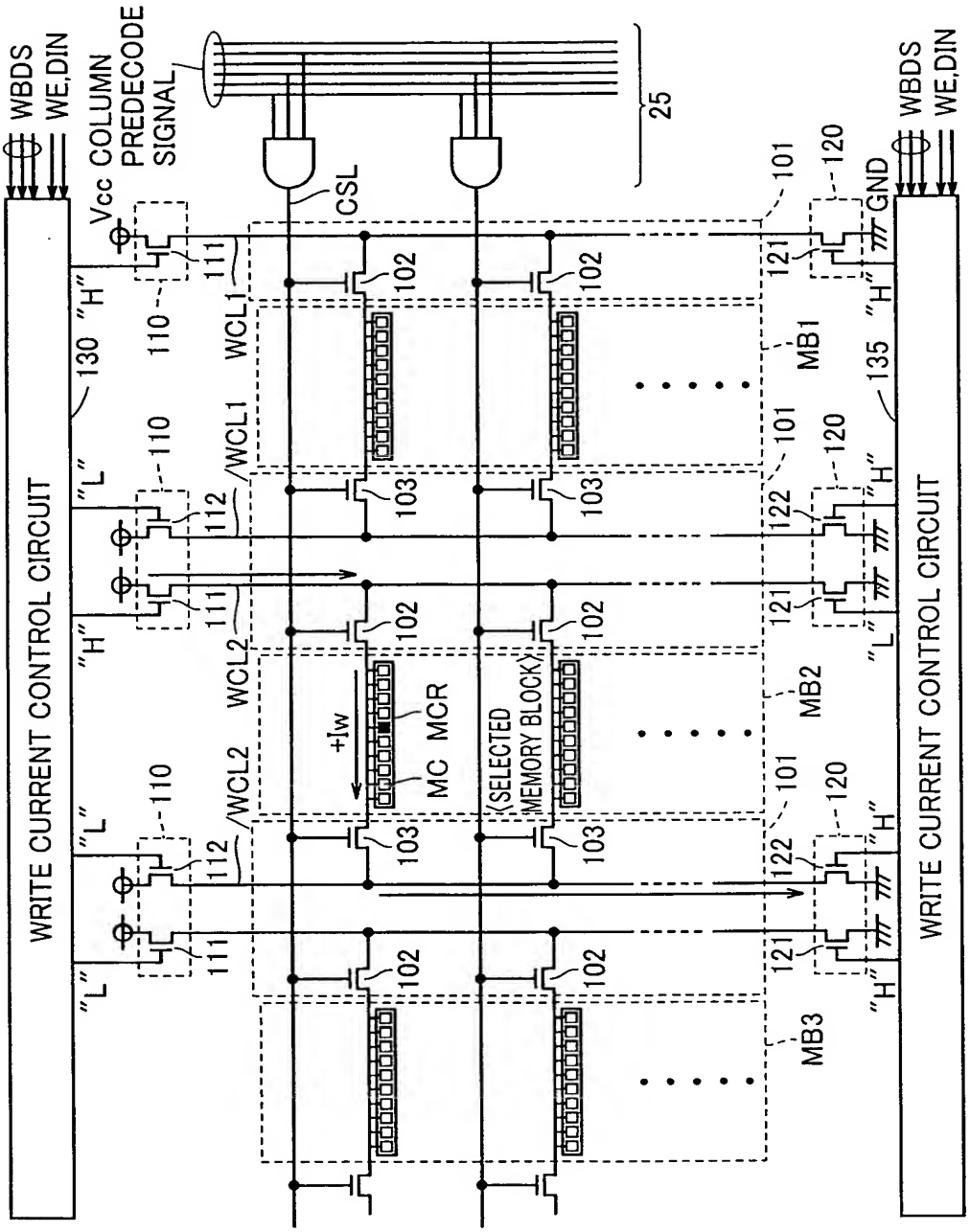
WBDS
WE,DIN
Vcc COLUMN PREDECODE SIGNAL
CSL
25
WRITE CURRENT CONTROL CIRCUIT
130
"H"
"L"
110
111
WCL1
/WCL1
112
WCL2
/WCL2
102
103
101
120
121
122
MB1
MB2
MB3
135
GND
+Iw
MC
MCR
(SELECTED MEMORY BLOCK)

FIG.11

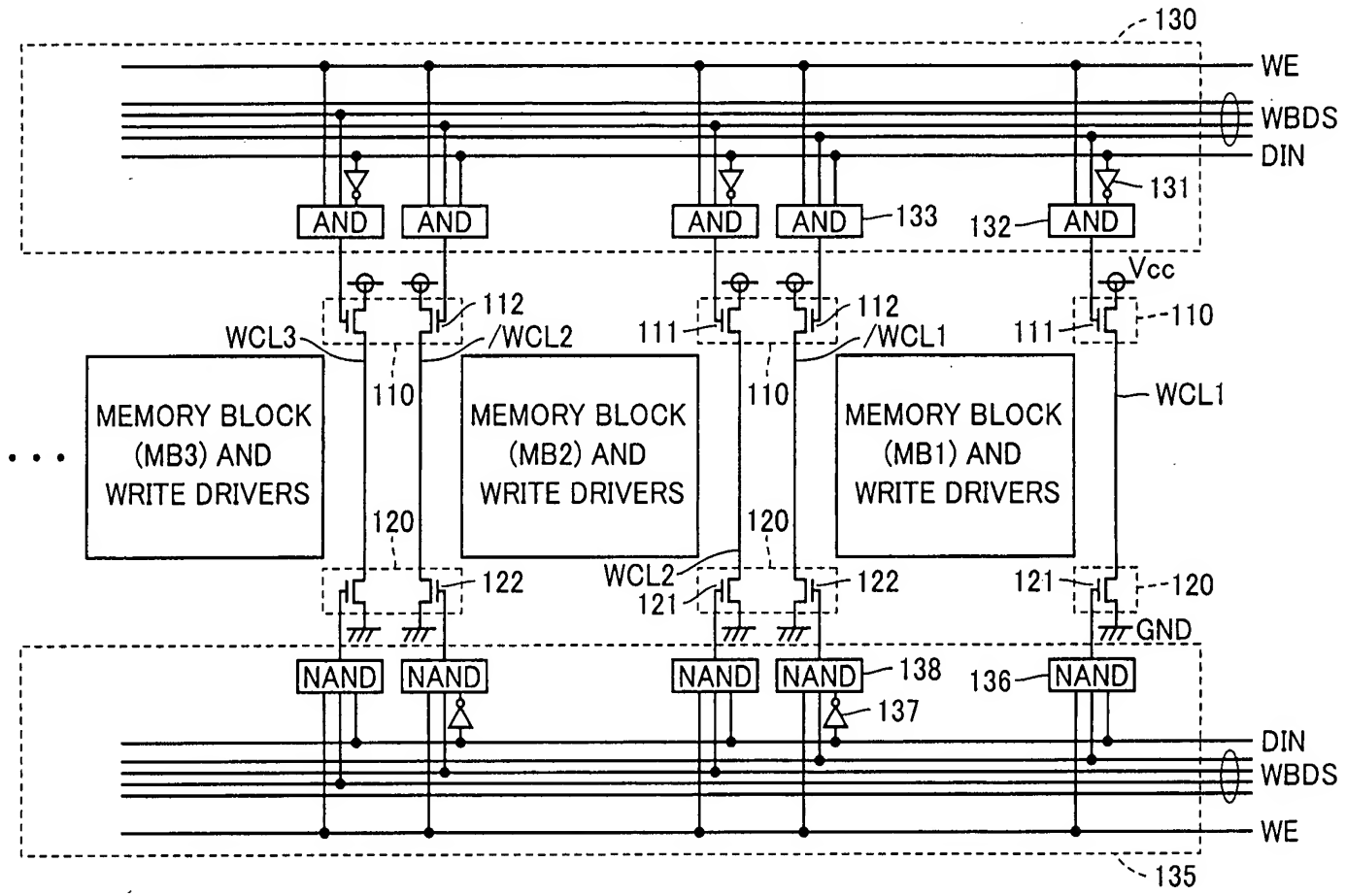
130
WE
WBDS
DIN
AND
AND
AND
AND
133
132
AND
131
Vcc
112
WCL3
/WCL2
111
112
/WCL1
111
110
110
110
WCL1
MEMORY BLOCK (MB3) AND WRITE DRIVERS
MEMORY BLOCK (MB2) AND WRITE DRIVERS
MEMORY BLOCK (MB1) AND WRITE DRIVERS
120
120
WCL2
122
121
122
121
120
GND
NAND
NAND
NAND
NAND
138
136
NAND
137
DIN
WBDS
WE
135

FIG.12

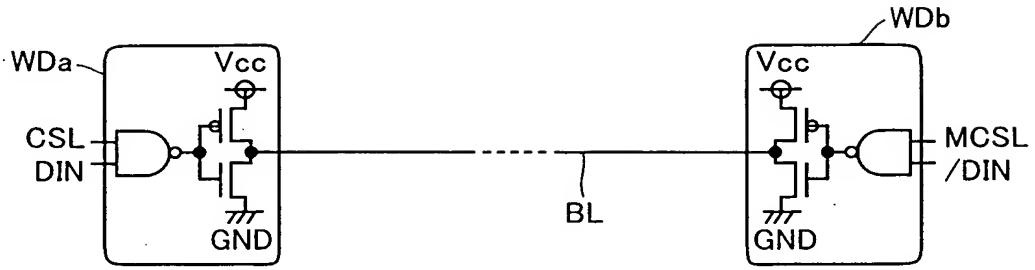

FIG.13

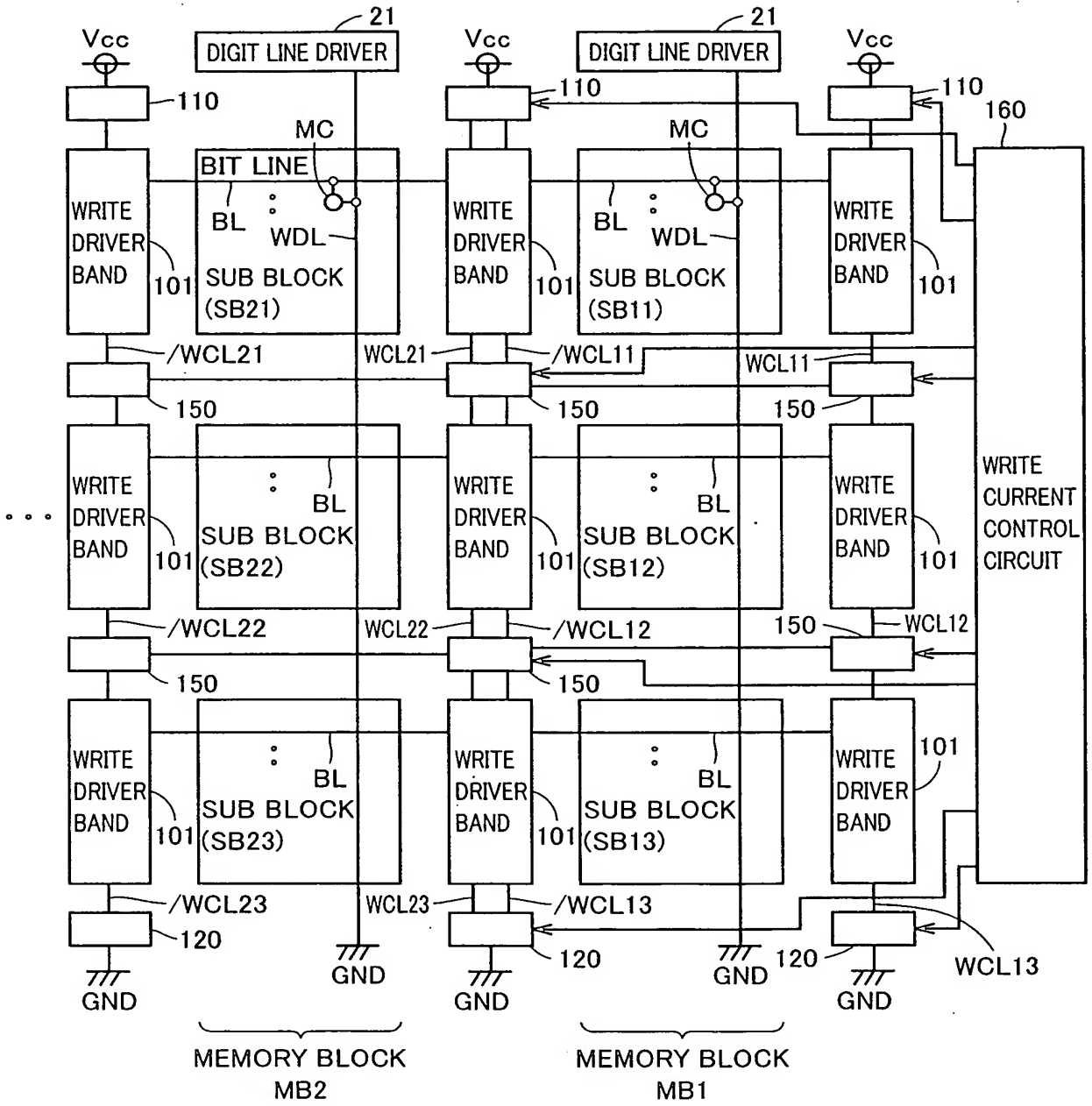
Vcc
21
DIGIT LINE DRIVER
110
MC
BIT LINE
BL
WDL
WRITE DRIVER BAND
101
SUB BLOCK (SB21)
SUB BLOCK (SB11)
SUB BLOCK (SB22)
SUB BLOCK (SB12)
SUB BLOCK (SB23)
SUB BLOCK (SB13)
/WCL21
WCL21
/WCL11
WCL11
150
/WCL22
WCL22
/WCL12
WCL12
/WCL23
WCL23
/WCL13
WCL13
120
GND
160
WRITE CURRENT CONTROL CIRCUIT
MEMORY BLOCK MB2
MEMORY BLOCK MB1

FIG.14

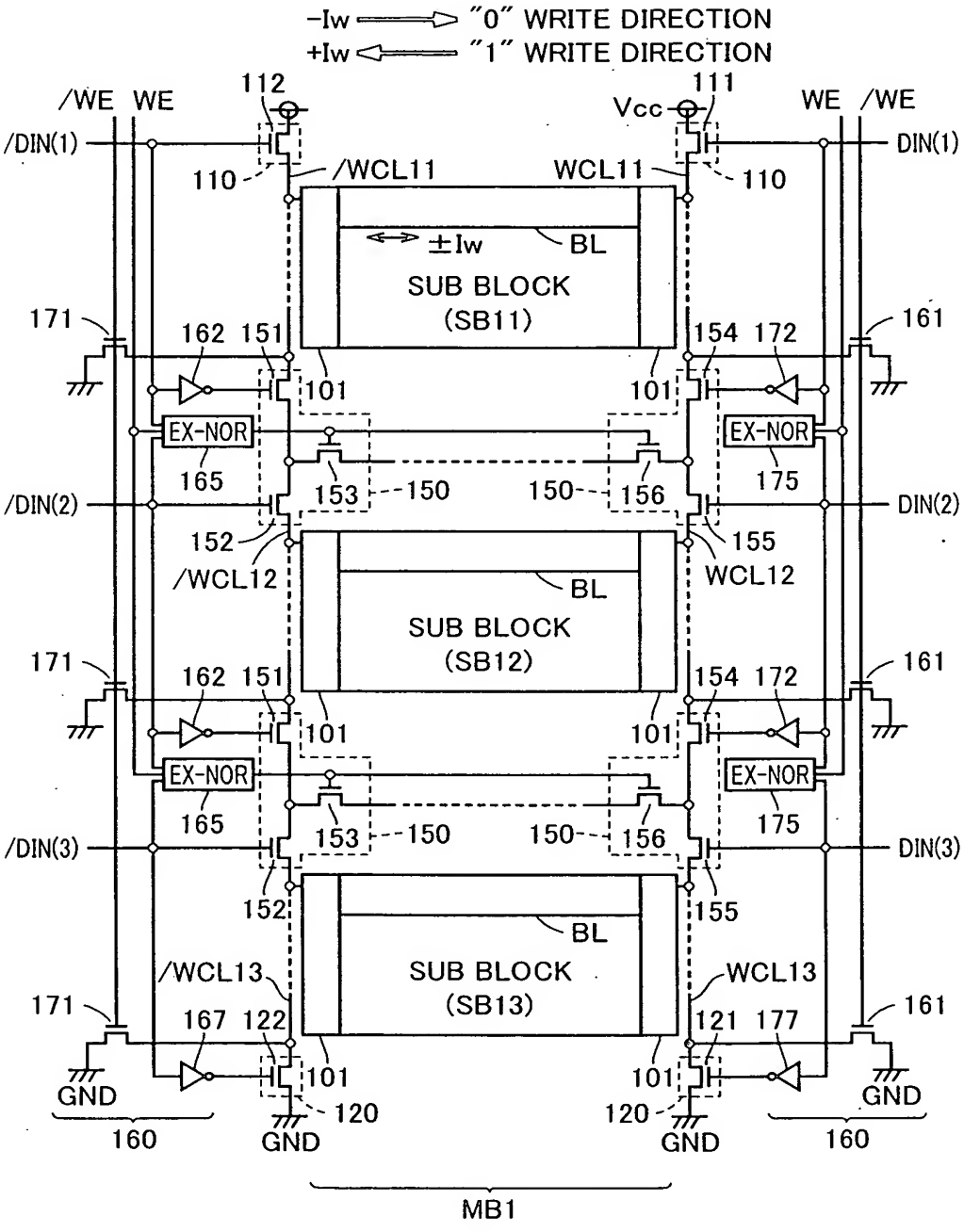
-Iw "0" WRITE DIRECTION
+Iw "1" WRITE DIRECTION
/WE
WE
112
Vcc
111
WE
/WE
/DIN(1)
DIN(1)
110
/WCL11
WCL11
110
±Iw
BL
SUB BLOCK
(SB11)
171
162
151
101
154
172
161
EX-NOR
165
153
150
150
156
175
/DIN(2)
DIN(2)
152
/WCL12
155
WCL12
BL
SUB BLOCK
(SB12)
171
162
151
101
154
172
161
EX-NOR
165
153
150
150
156
175
/DIN(3)
DIN(3)
152
155
BL
/WCL13
SUB BLOCK
(SB13)
WCL13
171
167
122
101
121
177
161
GND
120
GND
GND
120
GND
160
160
MB1

FIG.15

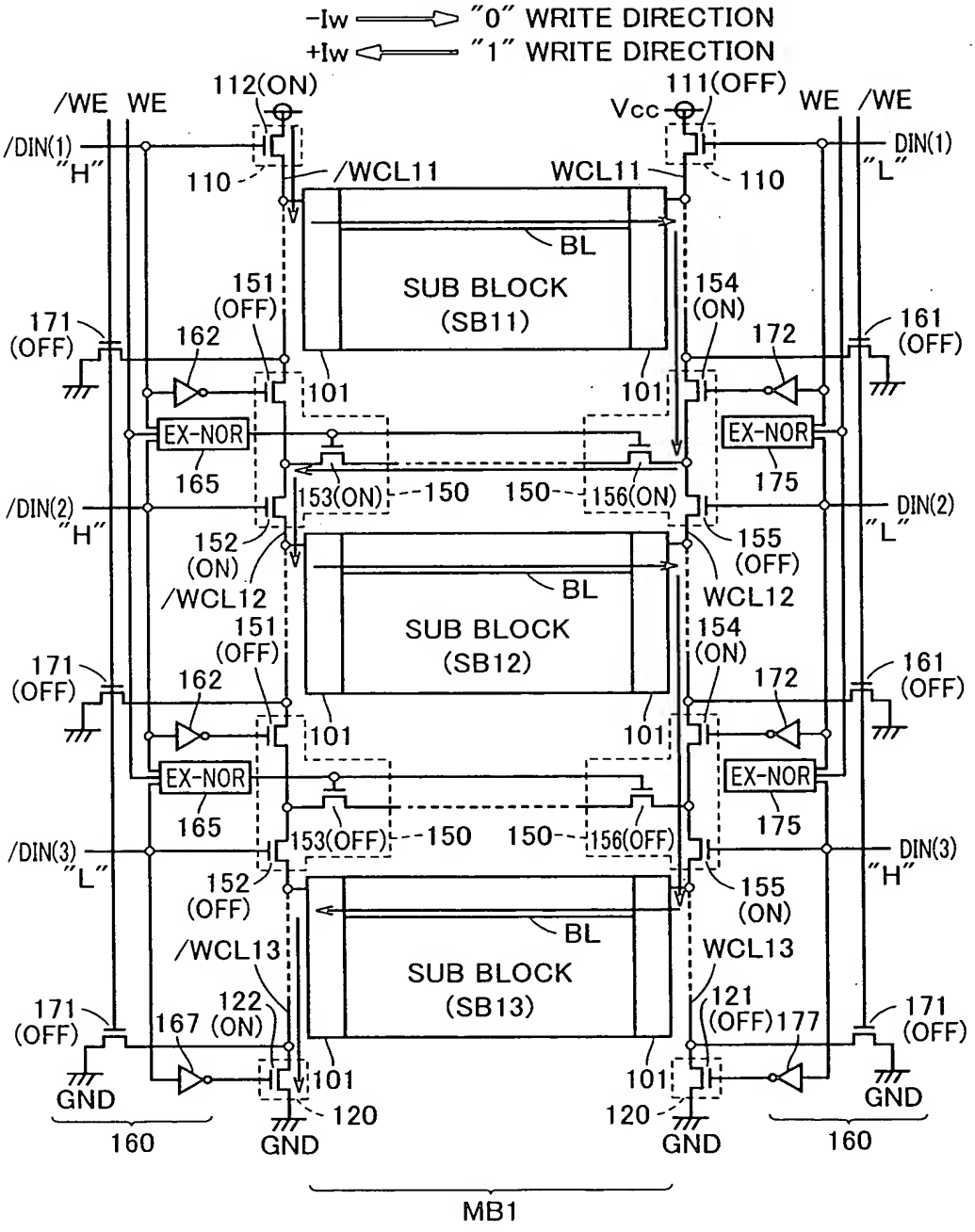
-Iw "0" WRITE DIRECTION
+Iw "1" WRITE DIRECTION
/WE
WE
112(ON)
111(OFF)
Vcc
/DIN(1)
"H"
DIN(1)
"L"
110
/WCL11
WCL11
BL
SUB BLOCK
(SB11)
151
(OFF)
154
(ON)
171
(OFF)
162
172
161
(OFF)
101
EX-NOR
165
175
153(ON)
150
156(ON)
/DIN(2)
"H"
DIN(2)
"L"
152
(ON)
155
(OFF)
/WCL12
WCL12
SUB BLOCK
(SB12)
153(OFF)
156(OFF)
/DIN(3)
"L"
DIN(3)
"H"
152
(OFF)
155
(ON)
/WCL13
WCL13
SUB BLOCK
(SB13)
122
167 (ON)
121
(OFF)
177
GND
120
160
MB1

FIG.16 PRIOR ART

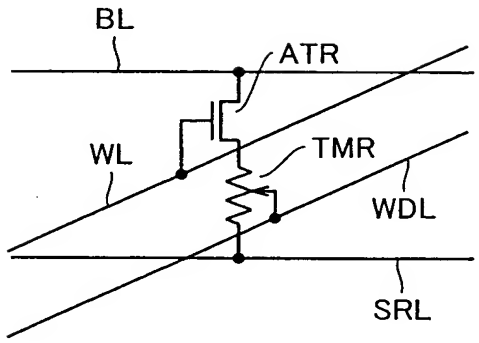

FIG.17 PRIOR ART

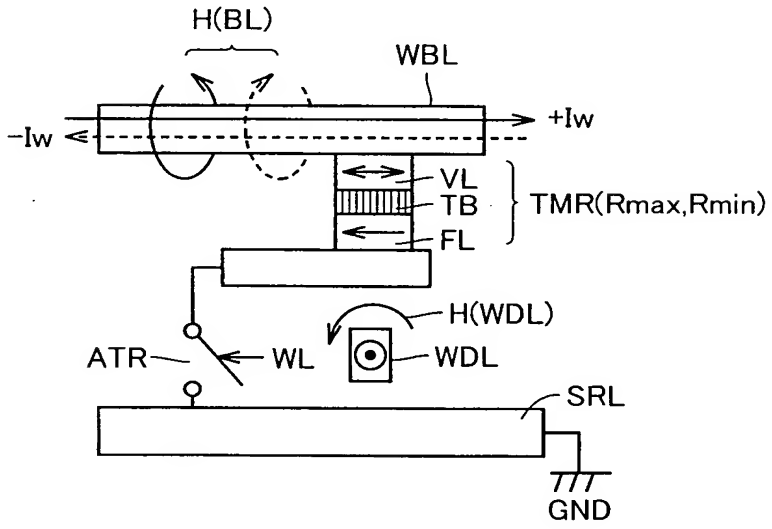

FIG.18 PRIOR ART

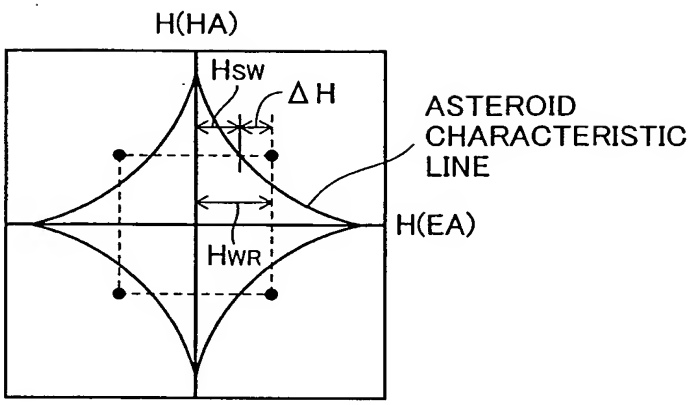

FIG.19 PRIOR ART

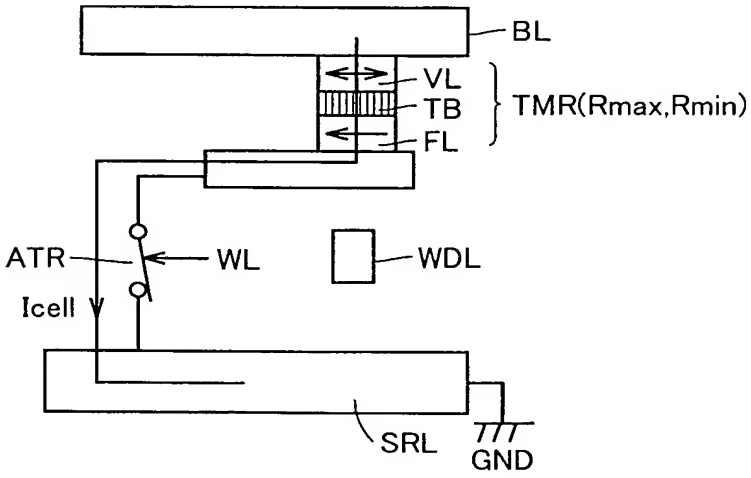
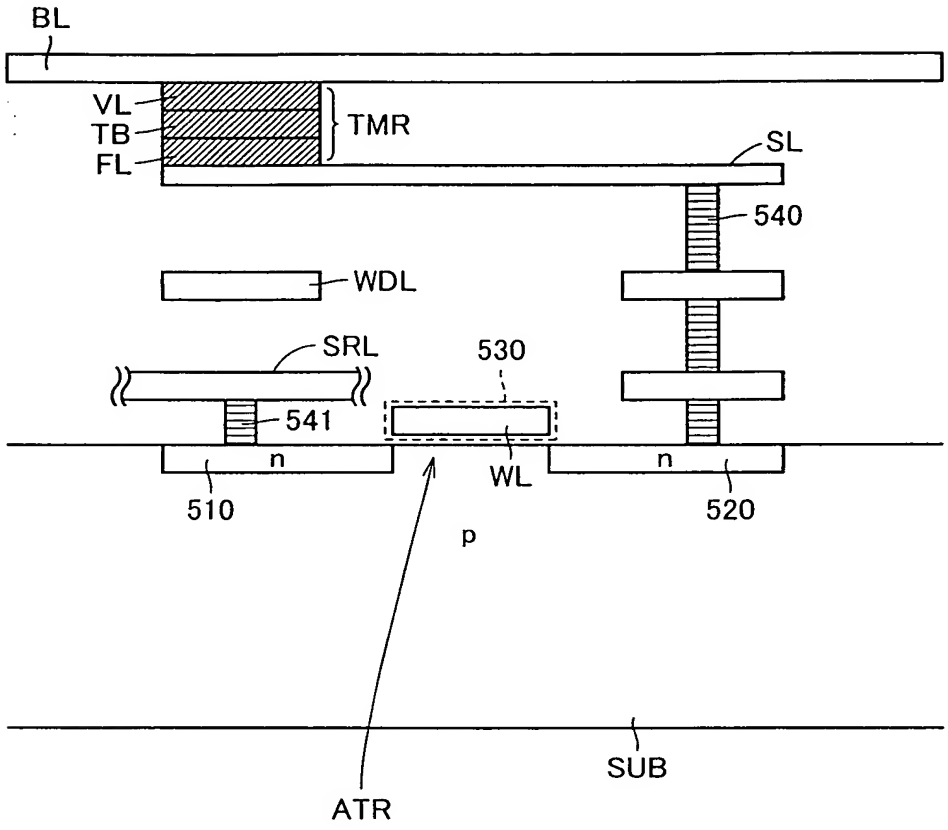
FIG.20 PRIOR ART